IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lin et al. **Examiner**: Doan, Duc T.

Serial No: 10/008,872 **Art Group**: 2188

Filing Date: November 8, 2001 **Docket No**: BP 1907

Title: MASTER TO MULTI-SLAVE ASYNCHRONOUS TRANSMIT FIFO

Date: April 17, 2008

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SECOND SUPPLEMENTAL APPEAL BRIEF
PURSUANT TO 37 C.F.R. § 41.37

Subsequent to the Final Office Action, a Notice of Appeal with a Pre-Appeal Brief was filed and received on July 12, 2007. The Pre-Brief Appeal Panel issued a Notice of Panel Decision having a mailed date of September 27, 2007, with an indication to proceed to the Board of Patent Appeals and Interferences, creating an Appeal Brief Due date, with an extension of time including appropriate fees, to now November 27, 2007. MPEP §§ 710.05, 1206.

A "Notification Of Non-Compliant Appeal Brief" had been issued having a mailed date of January 4, 2008 (hereinafter "Notice"). A supplemental appeal brief was tendered in response on February 2, 2008 within the time period permitted.

A further "Notification Of Non-Compliant Appeal Brief" had been issued having a mailed date of March 17, 2008 (hereinafter "Second Notice"), noting that the "Summary of the Claimed Subject Matter does not precisely map each limitation of the independent claim to the specification . . . ." (Second Notice at page 2). Responsive to the Second Notice, Appellant has

set out the claim elements noted, and referenced the elements to the Specification and to the Drawings in this Second Supplemental Appeal Brief, which is tendered within the period for response.

Accompanying the earlier Brief in Support of an Appeal were the necessary fees. If any petition fee for an extension of time or any other additional fee is required, the undersigned attorney directs the office to debit such fee from deposit account number 50-2126.

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A. Real Party in Interest

All rights to the above referenced patent application have been assigned to:

Broadcom Corporation
5300 California Avenue
Irvine, California 92617

B. Related Appeals and Interferences

There are no known other appeals or interferences that would directly or indirectly affect the Board's decision in the present appeal.

C. Status of the Claims

The Notice of Non-Compliant Amendment stated that the "status of claims is incorrect. The pending claims are 1, 3, 5-7, 11-17 and 20-22." (Notice at page 2).

Appellant had set out in its Appellant's Brief, filed November 2, 2007, that claims 1, 3-7, 11-17 and 20-22 are pending. Appellant had further noted that Claims 2, 4, 8-10, 18, and 19 had been earlier cancelled without prejudice. Accordingly, in view of the canceled claims, that Claims 1, 3, 5-7, 11-17 and 20-22 are being appealed.

In this regard, Appellant notes that Claims 1, 3, 5-7, 11-17 and 20-22 stand rejected as being unpatentable under an obviousness basis. In the Final Office Action mailed April 13, 2007, [hereinafter Final Office Action]), the rejection recited that:

> Claims 1, 3, 5-7, 11-17, 20, 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Published Application 2002/0183013 to Auckland et al ("Auckland"), in view of US Patent No. 5,968,143 to Chisholm et al ("Chisholm"), and further in view of U.S. Patent No. 6,434,630 to Micalizzi Jr, et al ("Micalizzi").
>
> Claim 21 was rejected under were rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland, Chisholm, Micalizzi, and in view of U.S. Published Application No. 2002/0009075, to Fesas, Jr. ("Fesas").

D. Status of Amendments

The "Notification of Non-Compliant Appeal Brief," having a mailed date of January 4, 2008, recited that "[a]t least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment." (*See* Notice at page 2).

Set forth in the initial filing of the Appeal Brief, Appellant noted that subsequent to the Final Office Action, a Notice of Appeal with a Pre-Appeal Brief was filed on, and received, July 12, 2007. A Notice of Panel Decision from Pre-Appeal Brief Review was issued having a mailed date of September 27, 2007, with an indication to proceed to the Board of Patent Appeals and Interferences.

No other documents, or amendments, were filed subsequent to the final rejection, having a mailed date of April 13, 2007.

E. Summary of claimed subject matter

The present application 10/008,827 involves memory structure improvements addressing resource allotment and transmission delays present in wireless transmission environments, such as, for example, in master-to-multi-slave wireless transmission environments. (*See* Specification at p. 7, *ll.* 11-26 through p. 8, *ll.* 1-7).

Appellant's Specification recites, by way of example, that its "method is advantageous in that, when coupled with the described structures herein, it facilitates a FIFO architecture in a master-multi-slave environment in which the size of the FIFO structure is minimized because the FIFO structure is used to contain pointer addresses rather than actual blocks of data." (Specification at p. 16, *ll.* 4-19). For re-transmission flexibility, a "flexible structure is presented in which FIFO integrity or ordering may be achieved while minimizing the size of a FIFO memory structure." (Specification at p. 22, *ll.* 9-12).

The claims 1, 3, 5-7, 11-17 and 20-22 presented for appeal include three independent claims and twelve dependent claims, which are "construed to incorporate by reference all the limitations of the claim to which [they refer]." 35 U.S.C. § 112, ¶ 4.

Appellant's Independent Claim 1 recites, *inter alia*, a "*wireless transceiver device* [(reference 200 (Figure 2; Specification at page 12, *ll.* 22-25))], comprising: modulation circuitry [(references 224, 216 (Figure 2, Specification at page 13, *ll.* 16-19)] for modulating and demodulating signals that are transmitted over airwaves; frequency conversion circuitry [(references 232, 208 (Figure 2, Specification at page 13, *ll.* 21-23, 1-3))] for up converting and down converting between radio frequency signals and baseband frequency signals; digital-to-analog conversion circuitry [(references 212, 228 (Figure 2, Specification at page 13, *ll.* 7-9, 19-

23))] for converting from analog to digital and from digital to analog; a radio controller [(reference 220 (Specification at page 13, *ll.* 14-19))]; baseband processing circuitry [(reference 230 (Specification at page 14, *ll.* 7-17))] including a first in, first out (FIFO) memory structure [(reference 242 (Specification at page 14, *ll.* 9-11))] for storing addresses for accessing data blocks; and a plurality of command blocks [(reference character 620 (Figure 6; Specification at page 21, *ll.* 9-10); reference character 712 (Figure 7; Specification at page 23, *ll.* 12-14))] formed within a memory structure [(reference character 238 (Figure 2; Specification at page 14, *ll.* 7-9))], the command blocks [(reference character 620 (Figure 6; Specification at page 21, *ll.* 9-10); 712 (Figure 7; Specification at page 23, *ll.* 12-14))] *include addresses of data blocks* stored within random access memory [(reference characters 624-34 (Figure 6; Specification at page 21, *ll.* 10-13); reference character 712 (Figure 7; Specification at page 23, *ll.* 10-12))] and a memory portion for storing *an indicator* [(reference character 720 (Figure 7; Specification 23, *ll.* 21-25))] for indicating whether a command block of the plurality of command blocks [(reference character 620 (Figure 6; Specification at page 21, *ll.* 9-10); reference character 712 (Figure 7; Specification at page 23, *ll.* 12-14))] is in use." (emphasis added).

Appellant's Independent Claim 7 recites, *inter alia*, a "method for storing and transmitting data, comprising: storing a data block in random access memory [(reference 246 (Figure 2; Specification at page 14, *ll.* 11-17))]; and storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure [(reference 604 (Figure 6; Specification at page 21, *ll.* 6-8); step 312 (Specification at page 15, *ll.* 2-5; Figure 3))], the pointer includes an address of a command block [(Specification at page 15, *ll.* 5-8; *see, e.g.,* Figures 3, 7)]; storing an address of the data block in the command block [(step 308 (Specification at page 14, *ll.* 26 through page 15, *ll.* 1-1-2; Figure 3))]; and *setting an indicator signal* in a defined memory

location [(step 316 (Specification at page 15, *ll.* 8-10; Figure 3))], wherein the indicator signal indicates that the data block address stored in the command block is for data *that has yet to be successfully transmitted and that the command block is busy* [(Specification at page 23, *ll.* 21-25)]." (emphasis added).

Appellant's Independent Claim 17 recites, *inter alia*, a "memory structure [(Figure 6; Specification at page 21, *ll.* 4-6; Specification at page 11, *ll.* 21-24)] formed within a baseband processing system [(reference 230 (Figure 2; Specification at page 14, *ll.* 7-17))], comprising: a random access memory portion [(reference 246 (Figure 2; Specification at page 14, *ll.* 11-14))] for storing data blocks [(reference 640-50 (Figure 6; Specification at page 21, *ll.* 13-16))] that are to be transmitted in a first in, first out (FIFO) order [(reference 636 (Figure 6; Specification at page 25, *ll.* 25))]; and a FIFO memory structure [(reference 242 (Figure 2; Specification at page 14, *ll.* 9-11))] for storing pointers [(reference 604 (Figure 6; Specification at page 21, *ll.* 6-10))] that correspond to the data blocks [(references 640-50 (Figure 6; Specification at page 21, *ll.* 13-16))] stored in the random access memory portion [(reference 246 (Figure 2; Specification at page 14, *ll.* 14-17))]; a plurality of command blocks [(reference 712 (Figure 7; Specification at page 23, *ll.* 10-15))] defined within the random access memory portion [(reference 246 (Figure 2; Specification at page 14, *ll.* 14-17))] wherein *each command block is for specifying an address of a data block that is to be transmitted* [(Specification at page 16, *ll.* 1-4; *id.* at page 24, *ll.* 5-18)]; and a defined memory portion for storing *command block indicators* for each command block [(reference 720 (Figure 7; Specification at page 23, *ll.* 21-25))], wherein the command block indicators specify whether its corresponding command block includes the address of a data block that has *yet to be transmitted successfully* [(Specification at page 24, *ll.* 2-5)]." (emphasis added).

F. Grounds of rejection to be reviewed on Appeal

Appellant presents for review the rejection of its claims 1, 3, 5-7, 11-17 and 20-22, in which claims 1, 3, 5-7, 11-17, 20, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Published Application 2002/0183013 to Auckland et al ("Auckland"), in view of US Patent No. 5,968,143 to Chisholm et al ("Chisholm"), and further in view of U.S. Patent No. 6,434,630 to Micalizzi Jr, et al ("Micalizzi").

Appellant's Claim 21, which depends indirectly from Independent Claim 17, was rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland, Chisholm, Micalizzi, and in view of U.S. Published Application No. 2002/0009075, to Fesas, Jr. ("Fesas").

G. Argument

1. The cited references of Auckland, Chisholm, and Micalizzi and/or Fesas lack some suggestion or motivation for their combination and/or *lack* the necessary teaching or suggestion of all of Appellant's claim limitations

In general, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Although the Supreme Court, in re-confirming the *Graham* factors, had admonished the use of the teaching-suggestion-motivation (TSM) test as an end of the obviousness inquiry, "[the Court] also recognized that [the teaching-suggestion-motivation (TSM) rationale] was one of a number of valid rationales that could be used to determine obviousness." MPEP § 2143 at 2100-118 (Rev. 6, Sept. 2007). Under this rationale, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Also, a finding is to be articulated that there was a reasonable expectation of success. MPEP § 2143 (G) at page 2100-138 (Rev. 6, Sept. 2007).

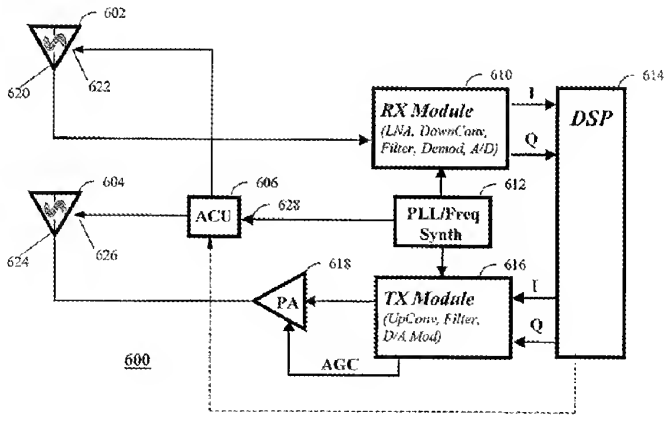
Further, all claim limitations must be considered. That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art. If an independent claim

is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03 at page 2100-142 (Rev. 6, Sept. 2007) (citations omitted).

a. ***the reconfigurable analog RF front end of* Auckland *does not recite memory structures for data transmission in a wireless environment***

Auckland relates to an "analog RF hardware in the front ends of personal and mobile communication radios that is reconfigurable for a variety of air interface standards." (Auckland ¶ 0048). Auckland does not recite data communication techniques, but instead reconfigurable analog front ends for radios.

With respect to reconfigurable analog radio front ends, Auckland simply recites *memory in an operational usage* for RF portion 600 *configurations*, which includes a "controller 614 may be dedicated to controlling the RF front end of the radio, including functions such as modulation, demodulation, encoding and decoding." (Auckland ¶ 0091). Figure 6 of Auckland illustrates an reconfigurable "analog front end of a radio device:"



(Auckland ¶ 0063). "In a software definable radio, where the radio hardware is fixed but may be customized by on-board software during operation [via the ACU 606] to allow the radio to operate in conjunction with a particular air interface standard or on a particular frequency band,

the customization operation may be controlled by the [ACU 606 implemented in the] controller 614." (Auckland ¶ 0091) (emphasis added).

The Final Office Action noted that "Auckland does not expressly disclose the claim's detail of associating data structures for storing data/commands as recited in the claim." (Final Office Action at p. 8). Indeed, Auckland pays passing, if any, tribute to data access (*see, e.g.*, Auckland ¶ 0003 ("the controller 614 is embodied as a digital signal processor (DSP) and operates in conjunction with data and instructions stored in memory."), ; Auckland recites antenna configuration techniques (see, e.g., Auckland Claim 1); *Id.* ¶ 0143 ("Other components of the radio may access data in the memory over a system bus or other communication means.").

Appellant respectfully submits that the Office Action uses the radio corollary in Auckland for the hypothetical combination of the cited references, but simply, Auckland does not recite an interaction of data memory and data transmission as set forth in Appellant's claimed invention.

b. ***the command block transfer device of* Chisholm *relates to command control across components of a computer device, not a wireless transceiver device with command blocks including addresses of data blocks in a wireless environment***

Chisholm relates to the "transfer of command blocks between two processing units communicating over an expansion bus." (Chisholm 1:16-17). In this regard, Chisholm's Summary of the Invention recites a "*command block transfer controller* [that] is *responsive to the transfer start signal* written by the host processing unit to start a command transfer for retrieving a command block from a corresponding host memory portion without local processing unit intervention." (Chisholm 3:1-4) (emphasis added).

Further, the device of Chisholm relates to the handling of the command blocks to local processing sides within a personal computer, not with data handling for wireless transmission. The FIFO buffer 326 of Chisholm does not provide "a first in, first out memory structure for storing addresses for accessing data blocks" as set out in Appellant's claimed invention.

For example, Chisholm recites that "[during] a *command block transfer* from the host processing side 110 to the local processing side 120, the FIFO buffer 326 receives and temporarily stores the *command block* from the host DMA state machine 322 and provides such *temporarily stored command block* to the local DMA state machine 324 to be stored in a *command block portion* of the local memory." (Chisholm 5:16-22). Figure 3 of Chisholm depicts a "computer system" with FIFO buffer 326:

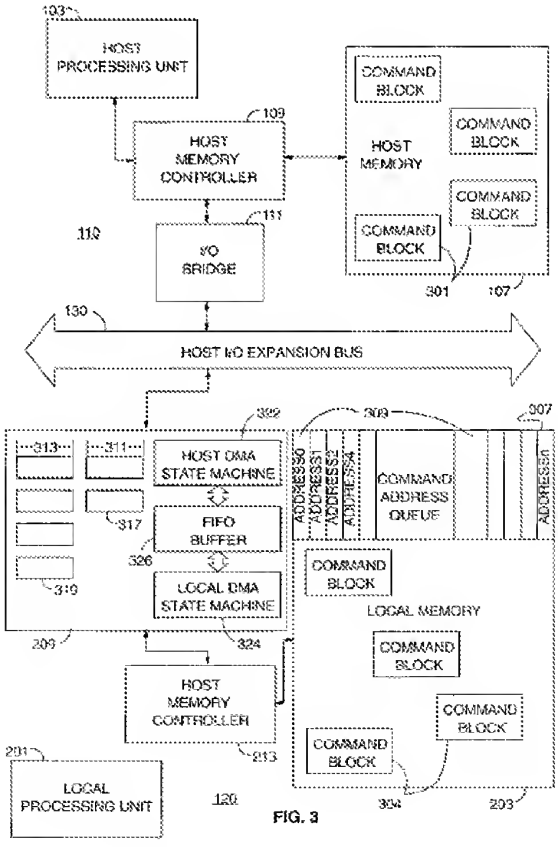


FIG. 3

The Chisholm command block "includes a command portion and a command address portion appended thereto." (Chisholm Claim 2). The "command address portion [of Chisholm] includes a chain enable information indicating whether another command block is chained to the transferred command block."

In other words, Chisholm recites that its command blocks pertain to command control between components of a personal computer. The disparate Chisholm command blocks do not include "addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use." (*see, e.g.,* Appellant's Claim 1; Specification at page 9, *ll.* 18-21).

c. ***the host adaptor device of* Micalizzi *recites interrupt management techniques, not the use of command blocks with addresses of data blocks and indicators for command blocks in a wireless environment***

Micalizzi relates "to a host adapter which reduces the number of input/output (I/O) completion interrupts generated from the host adapter to a host microprocessor." (Micalizzi 1:9-12). Figure 1 of Micalizzi "illustrates a compute system comprising a host computing system, a number of peripheral I/O devices and a host adapter board:"

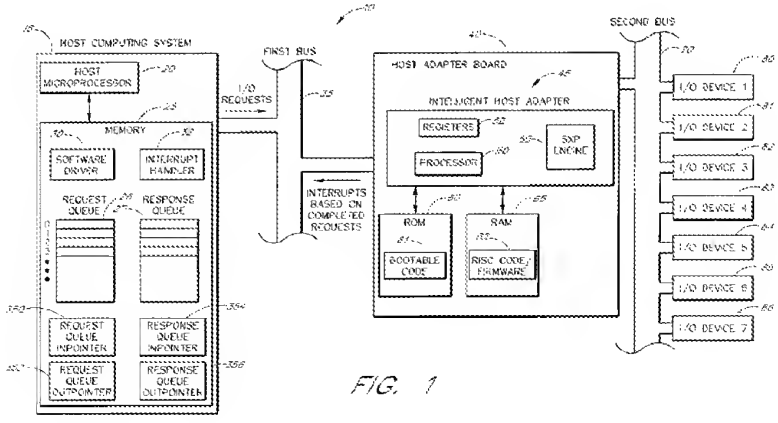


FIG. 1

(Micalizzi 4:42-45). The host adapter of Micalizzi seeks to increase processor performance by "combining successful I/O completion reports and reducing the number of interrupts [by] the host adapter [reducing] the overhead incurred in servicing interrupts for successfully completed I/O requests. This reduces the amount of processing time (`I/O bound` time) and power spent by the host microprocessor in *processing interrupts from the adapter*, and creates more time and power for the host microprocessor to *process user applications*." (Micalizzi 2:5-15). Micalizzi does not address command blocks with addresses of data blocks and indicators for command blocks as set forth in Appellant's claimed invention.

d. Fesas *recites address translation overhead reduction, not the use of command blocks with addresses of data blocks and indicators for command blocks in a wireless environment*

The Final Office Action noted that neither Auckland, Chisholm, nor Micallizzi recited specific command block lengths. In this regard, Fesas was cited as having a command block data structure having a length of 4 bytes.

Fesas relates to a "method and an apparatus for transferring data between a computer system and a network interface card that avoids virtual-to-physical address translations." (Fesas, Abstract). Fesas notes that the "advent of computer networking has given rise to devices that connect computer systems to packet-switched data networks. These devices . . . typically include interfaces to both the computer system and the packet-switched data network, as well as a buffer memory for buffering packets of data in transit between the computer system and the packet-switched data network." (Fesas ¶ 0004). In this regard, Fesas recites that "[w]hat is needed is performing DMA between a computer system and NIC which is free from the overhead of performing virtual to physical address translations . . . ." (Fesas ¶ 0009). Appellant respectfully

submits that Fesas does not recite memory structure improvements addressing resource allotment and transmission delays present in wireless transmission environments.

2. prior art corollaries from disjointed art references were collected and then, by improperly using Appellant's claimed invention as the blueprint, improperly combined

The Federal Circuit has stated that "virtually all [inventions] are combinations of old elements." *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 698 (Fed. Cir. 1983); *see also Richdel, Inc. v. Sunspool Corp.*, 714 F.2d 1573, 1579-80 (Fed. Cir. 1983) ('Most, if not all, inventions are combinations and mostly of old elements.'). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.' *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570 (Fed. Cir. 1996). To prevent the use of hindsight based on the invention to defeat patentability of the invention, [the Federal Circuit] requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

The Federal Circuit has recently bolstered its position opposing hindsight to substantiate rejections under Section 103, in which, "as the Supreme Court suggests, a flexible approach to the [Teaching, Suggestion, Motivation] test prevents hindsight and focuses on evidence before

the time of invention, without unduly constraining the breadth of knowledge available to one of ordinary skill in the art during the obviousness analysis." *In re Translogic*, 2007 U.S. App. LEXIS 23969 (Fed. Cir. Oct. 12, 2007) (referring to *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)); *see* MPEP § 2142, p. 2100-125 ("To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. . . .").

The Final Office Action collected "prior art corollaries" from the reconfigurable analog front-end of Auckland, from the intra-device "command block" transfer device of Chisholm, and from the host adapter of Micalizzi. Then, with the mix of disjointed transceiver, FIFO, and command block elements, the Final Office Action used "the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention." Further, the address translation overhead reduction of Fesas was cited for byte lengths.

Taking the cited references as presented, Appellant respectfully submits that no reasoning was provided that "the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

Appellant respectfully submits that a *prima facie* case of obviousness had not been set out. There is no suggestion or motivation to modify the reconfigurable RF front end of Auckland with the intra-device "command block" transfer of Chisholm, and further with the interrupt reduction of Micalizzi and/or address translation overhead reduction of Fesas to achieve

Appellant's claimed invention. Further, a *prima facie* showing of obviousness has not been established because the cited references do not teach or suggest all the limitations of Appellant's claimed invention as required.

G. Conclusions

For the above-provided reasons, the Appellant respectfully requests that all of the rejections of the Final Office Action be overturned and that the claims in the present application be allowed to issue.

Respectfully submitted,

Date: April 17, 2008 April 17, 2008 **/Kevin L. Smith/**

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H. Claims Appendix

1. (Previously Presented) A wireless transceiver device, comprising:

modulation circuitry for modulating and demodulating signals that are transmitted over airwaves;

frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals;

digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog;

a radio controller;

baseband processing circuitry including a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks; and

a plurality of command blocks formed within a memory structure, the command blocks include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

Claim 2. (Cancelled)

3. (Previously Presented) The wireless transceiver device of claim 1 wherein the FIFO memory structure includes pointers that define addresses of the command blocks.

Claim 4. (Cancelled)

5. (Previously Presented) The wireless transceiver device of claim 1 wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry.

6. (Previously Presented) The wireless transceiver device of claim 1 wherein the frequency conversion circuitry converts directly between radio frequency and baseband.

7. (Previously Presented) A method for storing and transmitting data, comprising:

storing a data block in random access memory; and

storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure, the pointer includes an address of a command block;

storing an address of the data block in the command block; and

setting an indicator signal in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data that has yet to be successfully transmitted and that the command block is busy.

Claims 8-10. (Cancelled)

11. (Previously Presented) The method of claim 7 wherein an address for a data block is only stored in a command block if the indicator signal reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted.

12. (Previously Presented) The method of claim 7 further comprises:

evaluating the command block address included within the FIFO pointer.

13. (Previously Presented) The method of claim 12 further comprises:

examining the contents of the command block specified by the pointer to determine a data block address.

14. (Previously Presented) The method of claim 13 further comprises:

evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size.

15. (Previously Presented) The method of claim 14 further comprises:

retrieving an amount of data corresponding to the data block size and transmitting that data to a radio modem for transmission over wireless airwaves.

16. (Previously Presented) The method of claim 15 further comprises:

resetting the indicator signal if the transmission was successful.

17. (Previously Presented) A memory structure formed within a baseband processing system, comprising:

a random access memory portion for storing data blocks that are to be transmitted in a first in, first out (FIFO) order; and a FIFO memory structure for storing pointers that correspond to the data blocks stored in the random access memory portion;

a plurality of command blocks defined within the random access memory portion wherein each command block is for specifying an address of a data block that is to be transmitted; and

a defined memory portion for storing command block indicators for each command block, wherein the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be transmitted successfully.

Claims 18-19. (Cancelled)

20. (Previously Presented) The memory structure of claim 17 wherein the defined memory portions for storing the command block indicators are each one bit in length.

21. (Previously Presented) The memory structure of claim 17 wherein the command blocks defined within the random access memory portions are each four bytes in length.

22. (Previously Presented) The memory structure of claim 17 wherein the FIFO memory structure defines a plurality of FIFO memory blocks wherein each FIFO memory block relates to data blocks that are to be transmitted to a particular device.

I. Evidence Appendix

No Evidence Submitted.

J. Related Proceedings Appendix

No Related Proceedings